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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,076	10/04/2005	Andrei Terechko	NL 030344	8796

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EXAMINER	
VICARY, KEITH E	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,076	TERECHKO, ANDREI	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are pending in this application and presented for examination.

2. Claims 1-5 are amended and claims 6-8 are added by an amendment filed 3/15/2007.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed, for example, the pipeline registers.

4. Although the examiner is no longer objecting to the lack of section headings in the instant specification, the examiner would like the applicant to reconsider adding in section headings, as the use of section headings enables more efficient searching by examiners.

Claim Objections

5. Claim 5 is objected to because of the following informalities. Appropriate correction is required.

a. In claim 5, line 7, "register" should be "registers."

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

b. In claim 1, lines 9-10 and claim 5, lines 9-10, the applicant's amended claims disclose "said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters." It is indefinite as to how a pipeline register may solely provide a connection between any two of said clusters, as opposed to the connection between the instruction unit and the clusters, which is connected by both a pipeline register and respective control connections. Furthermore, it is indefinite as to if the same pipeline registers are being used as part of both the control connections and the data connections, or whether a subset of the pipeline registers are being used for one type of connection, and the remaining pipeline registers for the other type of connection.

i. Claims 2-4 and 6-8 are rejected for further failing to alleviate the rejection of claims 1 and 5 above.

Claim Rejections - 35 USC § 103

8. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, also in col. 7, lines 4-7, clustered processor), comprising a plurality of clusters each comprising at least one register file and at least one functional unit (Figure 12 shows clusters 108, which in col. 11, lines 7-8, show to contain ALUs, also col. 1, lines 43-45, execution units, register file; register files also in col. 3, lines 32-35); an instruction unit (IFD) for issuing control signals to said clusters (Figure 12, fetch and decode units 104 and 106, also col. 11, lines 3-4, fetch and decode unit; the control signals are inherent in D-H of Figure 12 and col. 11, line 65, instruction path), wherein said instruction unit is connected to each of said clusters via respective control connections (D-H of Figure 12 and col. 11, line 65, instruction path), and said pipeline registers being adapted to provide a dedicated direct signal connection between any two of said clusters (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity, requiring additional move instructions; col. 3, line 23-43 go into detail about the arrangement).

However, Batten does not disclose that one or more additional pipeline registers is arranged in said control connections depending on the distance between said instruction unit and said clusters.

On the other hand, Nickolls does disclose of one or more additional pipeline registers arranged in control connections depending on the distance between an instruction unit and clusters (col. 6, lines 1-45, pipeline registers; col. 21, lines 13-32

and col. 22, lines 30-42 and 56-62 shows the operation of the pipeline registers; col. 23, lines 13-16, shows multiple pipeline registers per path can be placed for time reasons; col. 59, lines 64-67, col. 60, lines 1-6, allow for different embodiments).

The teaching of Nickolls' of adding in pipeline registers to serve as intermediate points for signals allows for more flexibility in component density, allows for instruction synchronization, allows for greater overall improvements in performance by adding additional clusters/processors, and increases throughput of said signals (Nickolls, stated across col. 2, lines 30-36; col. 2, lines 54-57; col. 2, lines 60-64; col. 3, lines 55-64; col. 4, lines 1-14; col. 5, lines 51-64; col. 20, lines 11-31; col. 23, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals. Furthermore, it would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls fits into the environment of Batten as both are sending message bits/signals to destination processors/clusters. It would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls also works indiscriminate of whether control signals or data signals are passing through it.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the pipeline registers of Nickolls with

the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals.

9. Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, also in col. 7, lines 4-7, clustered processor), comprising a plurality of clusters each comprising at least one register file and at least one functional unit (Figure 12 shows clusters 108, which in col. 11, lines 7-8, show to contain ALUs, also col. 1, lines 43-45, execution units, register file; register files also in col. 3, lines 32-35); an instruction unit (IFD) for issuing control signals to said clusters (Figure 12, fetch and decode units 104 and 106, also col. 11, lines 3-4, fetch and decode unit; the control signals are inherent in D-H of Figure 12 and col. 11, line 65, instruction path), wherein said instruction unit is connected to each of said clusters via respective control connections (D-H of Figure 12 and col. 11, line 65, instruction path), and said pipeline registers being adapted to provide a dedicated direct signal connection between any two of said clusters (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity, requiring additional move instructions; col. 3, line 23-43 go into detail about the arrangement).

However, Batten does not disclose that one or more additional pipeline register is arranged in said control connections depending on the distance between said instruction unit and said clusters.

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The teaching of Nickolls' of adding in pipeline registers to serve as intermediate points for signals allows for more flexibility in component density, allows for instruction synchronization, allows for greater overall improvements in performance by adding additional clusters/processors, and increases throughput of said signals (Nickolls, stated across col. 2, lines 30-36; col. 2, lines 54-57; col. 2, lines 60-64; col. 3, lines 55-64; col. 4, lines 1-14; col. 5, lines 51-64; col. 20, lines 11-31; col. 23, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals. Furthermore, it would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls fits into the environment of Batten as both are

sending message bits/signals to destination processors/clusters. It would have been readily apparent to one of ordinary skill in the art at the time of the invention that the invention of Nickolls also works indiscriminate of whether control signals or data signals are passing through it.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the pipeline registers of Nickolls with the invention of Batten in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals.

10. Consider claims 2 and 6, Batten discloses said clusters are connected to each other via a point-to-point connection (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity, requiring additional move instructions; note that a fully connected structure is a type of point-to-point connection structure).

11. Consider claims 3 and 7, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

12. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

13. Consider claims 4 and 8, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

On the other hand, Pechanek does disclose that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate). Furthermore, it is noted that the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art.

Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs. Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that the disclosed bus of Pechanek also fits into the environment of Batten and Nickolls as both are related to communication architectures between a control unit and its corresponding clusters/processor elements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten

and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

Response to Arguments

14. Applicant's arguments filed 3/15/2007 have been fully considered but they are not persuasive. Therefore the rejection of the original claims is maintained.

15. In the remarks, applicants argued that the prior art of reference do not teach the newly added limitation in independent claims 1 and 5.

16. Examiner respectfully traverses applicant's remarks.

17. As explained above in the rejection of claims, the prior art of record does teach the newly added limitation in independent claims 1 and 5.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

c. Tudruj, "Embedded Cluster Computing through Dynamic Reconfigurability of Inter-Processor Connections," Proceedings of the NATO Advanced Research Workshop on Advanced Environments, Tools, and Applications for cluster Computing – September 01-06, 2001, also teaches the use of fully connected networks in cluster computing in section 2, paragraph 3.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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